A GaAs MCM Power Amplifier of 3.6 V Operation with High Efficiency of 49% for 0.9 GHz Digital Cellular Phone Systems

Kazuki Tateoka, Akihisa Sugimura, Hidetoshi Furukawa, Noriyuki Yoshikawa, and Kunihiko Kanazawa

Abstract— **An Extremely small GaAs PA (power amplifier) has been implemented using AlN multilayer MCM for 0.9 GHz digital cellular phones. The present PA exhibited high efficiency of 49% with drain supply voltage as low as 3.6V. This PA was designed to provide matching circuits with the maximum gain at the input side and the minimum intermodulation distortion at the output side. Nonlinear simulation result verifies that this matching condition provides the lowest $\pi/4$-shift QPSK distortion and indicates that the phase shift of the amplifier is mainly caused by source-drain resistance.**

I. Introduction

FOR THE APPLICATION of cellular phones, low drain voltage and high efficiency characteristics are strongly required especially for power amplifier in order to reduce the size and weight of phones and in order to enable long talk time. Moreover, the digital mobile radio service using $\pi/4$-shift QPSK signal needs low distortion characteristics for all components in the system. However, requirements for linear operation results in reducing the efficiency of power amplifier. The power amplifier module which consists of GaAs FET's has the advantage to attain high efficiency [1] and high linearlity characteristics. Although, the efficiency of power amplifier for $\pi/4$-shift QPSK digital signal in 0.9 GHz frequency band has been reported as low as about 40% even at high operating voltage such as 5.8V [2].

In this paper, we design high efficiency and low distortion GaAs MuMIC (multilayer microwave integrated circuit) power amplifier at low drain voltage for 0.9 GHz Japanese digital cellular phones. As is well known, the design of input and output matching circuits for GaAs FET's is important to attain high efficiency and low distortion performance. However, in the case of $\pi/4$-shift QPSK signal, it has been still discussed how to reduce the modulated distortion of FET's and how to design the matching circuits [2]–[4]. We discuss the design method to determine the matching circuit of the MuMIC power amplifier in order to achieve low distortion of $\pi/4$-shift QPSK signal with keeping high efficiency. The effect of nonlinear device parameters of GaAs FET's to the distortion of $\pi/4$-shift QPSK signal is discussed in this paper.

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The authors are with Matsushita Electronics Corporation, Electronics Research Laboratory, Takatsuki, Osaka, Japan.

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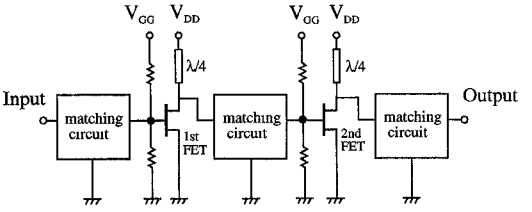

Fig. 1. The circuit diagram of GaAs MuMIC power amplifier.

II. Circuit Design

We design high efficiency and low distortion power amplifier operating at low drain voltage with the MCM (multichip module) structure. The circuit of MCM amplifier is designed to have two GaAs FET's and input and output matching circuits as shown in Fig. 1. The design method of matching circuits, which is important to obtain high efficiency and low distortion characteristics, is described in this section.

In the case of designing the amplifier for the $\pi/4$-shift QPSK modulation, the matching circuits of the power FET are separately designed at the input and output sides for high gain, high efficiency, and low distortion operation. To design the input circuit of the second stage FET, we measured characteristics such as gain and the variation of phase shift which is generated between the input and output sides of the FET with changing the input matching condition, by source-pull method. For this measurement, the output power P_{out} of the FET, which has the gate width of 27 mm, is fixed to be constant of 1.3 W at the frequency of 0.9 GHz. It is biased under conventional class-AB condition with drain supply voltage of 3.6 V. The output matching is fixed to give a low IM distortion during the measurement by the reason described in the following paragraph. The result is plotted in the Smith chart as shown in Fig. 2. The contour line of the gain and the phase shift indicates a different tendency. At the maximum gain matching point, the phase shift is about 0.8 deg./dB, that is considered to be small enough to suppress the phase distortion of $\pi/4$-shift QPSK signal [2]. In fact, the adjacent channel interference level of the $\pi/4$-shift QPSK signal is -53 dBc at ± 50 kHz apart from the center frequency. Consequently, we choose the input matching circuit to be this maximum gain matching point. The input matching circuit of the first stage FET is designed in the same way.

In order to design the output circuit, we estimate the characteristics of the second stage FET, such as the distortion of

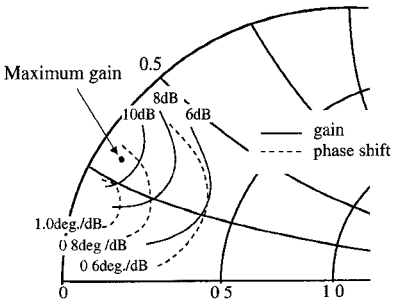

Fig. 2. Source-pull measurement result.

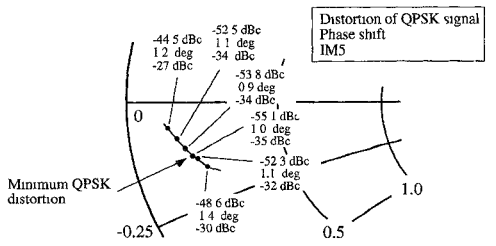

Fig. 3. Lord-pull measurement result.

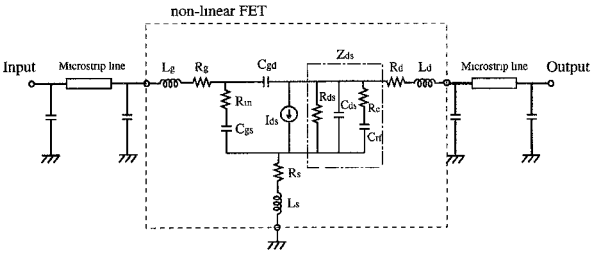

Fig. 4 GaAs FET equivalent circuit and input/output matching circuits used in the calculation.

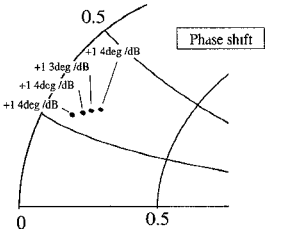

Fig. 5. Simulation result of phase shift with changing the impedance of input matching circuit.

the $\pi/4$-shift QPSK signal, IM (intermodulation) distortions, and the phase shift at the same matching condition using load-pull method. Fig. 3 shows the result of this measurement at the frequency of 0.9 GHz. The output power is fixed to be 1.3 W, and the power-added efficiency is kept to be constant for this measurement in order to use these data for the design of high efficiency power module. As shown in Fig. 3, among the measured high order IM distortions, the fifth order distortion IM5 shows the strongest relation with the distortion of the $\pi/4$-shift QPSK signal. The minimum IM5 matching offers the minimum distortion matching for the $\pi/4$-shift QPSK signal. The variation of phase shift also seems to be related with the distortion of the $\pi/4$-shift QPSK signal. However, the difference of the values of the phase shift at each matching condition is small enough. Therefore, we design the output matching circuit of the second stage to be the optimum IM matching condition.

The matching circuits of the first stage FET is designed almost in the same way. However, the distortion of the $\pi/4$-shift QPSK modulation of the output signal should be suppressed less than -62 dBc. Therefore, it is biased under class A condition.

III. Nonlinear Simulation Result

In order to analyze the cause of phase shift and IM distortions, we simulate the amplifier characteristics using the GaAs FET equivalent circuit and input/output matching circuits as shown in Fig. 4. The curtice cubic $I_{\rm ds}$ model [5] and other extracted device parameters from measurements are used. In this calculation, g_m which is derived from the $I_{\rm ds}$ equation and $C_{\rm gs}$ are taken into account as nonlinear factors. The nonlinear $C_{\rm gs}$ is expressed as a polynominal equation of $V_{\rm gs}$, which is fitted from C-V measurement data.

The phase shift and IM distortions are calculated by the harmonic balance method at fixed output power.

The phase shift is first calculated to make clear which device parameters cause the change of phase shift. Fig. 5 shows the calculation result of phase shift with changing the input matching condition. The output matching is fixed to offer the minimum IM5 distortion. There is only 0.1 deg./dB change in this range as shown in the Fig. 5. It can be considered that the device parameters at the input side such as $R_{\rm in}$ and $C_{\rm gs}$ do not affect the change of phase shift.

The device parameters of output side are examined next. The phase shift is calculated with changing $C_{\rm gd}$ and source-drain impedance $Z_{\rm ds}$ at the maximum gain input matching and the minimum IM5 output matching condition. The degree of $C_{\rm gd}$ and $Z_{\rm ds}$ effect is evaluated as a changing rate Δ phase-shift/Δ $C_{\rm gd}$ and Δ phase-shift/$\Delta Z_{\rm ds}$. The changing rate becomes -15% and 104%, respectively. It indicates that the phase shift strongly depends on these parameters. The source-drain impedance, in particular, affects the phase shift significantly. The source-drain impedance of power FET's used here is dominated by Rc among the four elements composing $Z_{\rm ds}$ in the frequency range of 0.9 GHz. Therefore, it can be said that the most important device parameter for the analysis of phase shift is source-drain resistance.

The simulation results including phase shift and IM5 with changing output matching condition are summurized in Fig. 6. At the matching point (A), IM5 becomes the minimum value of -36.4 dBc. This matching condition must offer the minimum $\pi/4$-shift QPSK distortion. As the matching point is changed, IM5 becomes larger as indicated by contour lines in the Smith chart. The tendency of IM5 change along the line having fixed efficiency coincides with the load-pull measurement result shown in Fig. 3. This means that the nonlinearity of g_m and $C_{\rm gs}$ which are taken into account in this calculation offers the cause of IM5 distortion. On the other hand, the phase shift shows the different tendency between the experiment and the calculation. It changes monotonously along the line of points shown in Fig. 6. We consider that the accurate modeling of

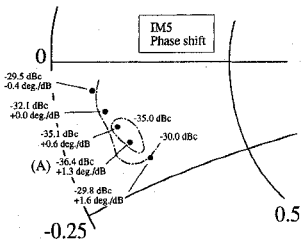

Fig. 6. Simulation result of IM5 and phase shift plotted in the Smith chart with changing the impedance of output matching circuit.

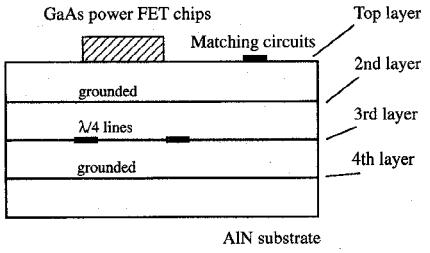

Fig. 7. Cross-sectional view of MuMIC power module.

nonlinearity of the source-drain resistance should be needed to analyze the phase characteristics. It will make it possible to obtain the expectation of various characteristics of the amplified signal of the $\pi/4$-shift QPSK modulation.

IV. MuMIC And FET Design

In this section, MuMIC structure are described. The MuMIC has AlN mutilayer MCM structure which is considered to be the most effective candidate for the future application of power devices. Fig. 7 shows the cross section of the MuMIC. It consists of 4 layers of AlN substrate. The material of AlN has the high dielectric constant ϵ_r of 8.8 enough for the use of 0.9 GHz frequency range and the thermal conductivity of 150 W/m · k which is advantageous for high power operation.

The $\lambda/4$ short stubs providing the bias circuits which occupy large circuit area are inserted in the third layer of the mutilayer structure, resulting in the reduction of the size of the MuMIC. The top and the third layer are separated by the grounded layer as shown in Fig. 7. The size of the MuMIC is miniaturized to be $11\times14\times3$ mm which is half that of conventional hybrid IC power amplifiers.

On the top layer, two GaAs chips, matching circuits, and gate bias circuits are composed. GaAs FET's used in this MuMIC power amplifier are designed to reduce the knee voltage V_k of DC drain current-voltage characteristics so as to avoid the decrease of power-added efficiency when the drain voltage becomes lower. The FET's are designed to have short gate length of 0.6 μm and highly doped N^+ layer at the source and drain contacts. Moreover, the doping profile of the active layer is adopted to reduce the on-resistance. Thus the V_k is reduced to be 1.5 V by about 30% in comparison with the one of the conventional FET's having the same I_{dss}. The gate width of the FET's of this MuMIC power amplifier are designed to be 4 mm and 27 mm, respectively, in order to obtain 1.3 W average output power of the $\pi/4$-shift QPSK

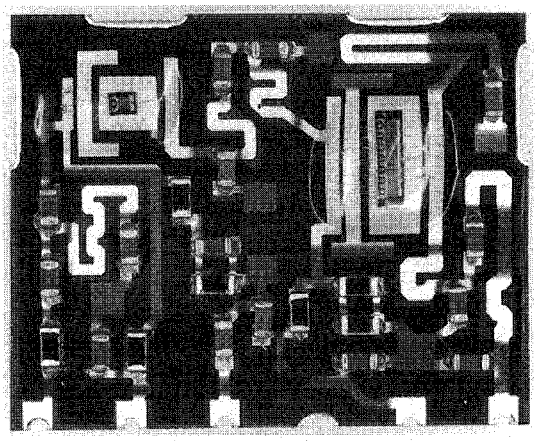

Fig. 8. Top view of the AlN MuMIC power amplifier.

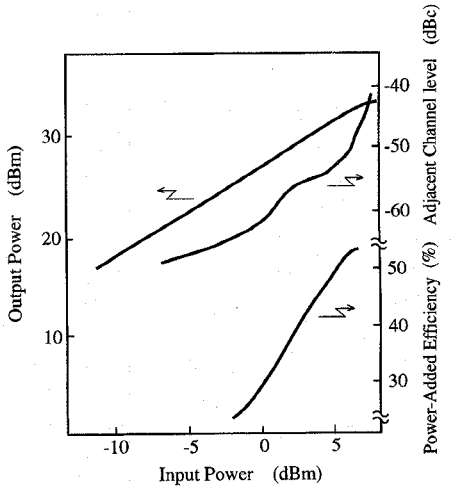

Fig. 9. RF characteristics of MuMIC power amplifier.

signal. These chips are directly mounted by AuSn solder. The matching circuits and gate bias circuits are fabricated by using the chip capacitors, resistors, and microstrip lines. The top view of the AlN MuMIC is shown in Fig. 8.

V. RF Characteristics

The input-output power characteristics of this MuMIC power module is shown in Fig. 9. The power-added efficiency and distortion level of the $\pi/4$-shift QPSK modulation are also measured and plotted. The high power-added efficiency of 49% at 1.3 W average output power of $\pi/4$-shift QPSK signal is obtained with the low supply voltage of 3.6 V at the frequency of 0.9 GHz. The modulated signal distortion is suppressed, so that the adjacent channel interference level at the ±50 kHz apart from the center frequency is lower than -50 dBc. The spectrum of the output QPSK signal of MuMIC power amplifier is shown in Fig. 10.

VI. Conclusion

The high efficiency GaAs power amplifier operating at low drain voltage of 3.6 V for 0.9 GHz Japanese digital cellular phones using $\pi/4$-shift QPSK signal with the MuMIC

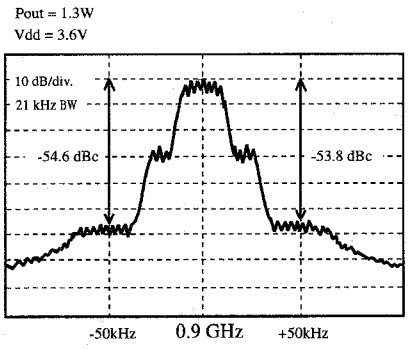

Fig. 10. Spectrum of the output QPSK signal of MuMIC power amplifier.

technology has been developed. The MuMIC has the AlN mutilayer MCM structure which is considered to be the most effective candidate for the future application of power devices. It consists of two GaAs power FET chips and matching circuits on AlN substrate which has the mutilayer structure. The size of the MuMIC is miniaturized as $11\times14\times3$ mm which is half that of conventional hybrid IC power amplifier. The design method of matching circuits is discussed. It is shown that the maximum gain matching for the input side and the minimum IM distortion matching for the output side are effective for the amplifier design of $\pi/4$-shift QPSK signal. The extremely high efficiency of 49% and low distortion characteristics with 1.3 W output power has been demonstrated with low supply voltage of 3.6 V at the frequency of 0.9 GHz. The nonlinear FET simulation has been performed, and the result shows that the nonlinearity of gm and C_{gs} affects the IM distortions, and the source-drain resistance is the main cause of phase shift between input and output signal.

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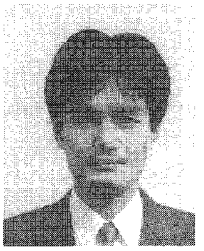
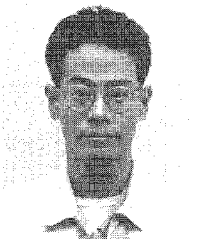


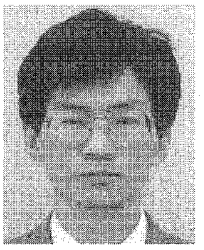
Kazuki Tateoka was born in Hiroshima, Japan. He received the B.S. and M.S. degrees in electronics engineering from Kyoto University, Kyoto, Japan, in 1984 and 1986, respectively.

In 1986, he joined Electronics Research Laboratory of Matsushita Electronics Corporation in Osaka, where he was engaged in the research and development of semiconductor laser diodes and other semiconductor optical devices. Since 1991, he has been in charge of the development of GaAs MESFET and GaAs power module.



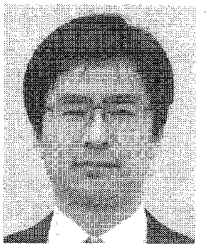
Akihisa Sugimura was born in Osaka, Japan. He received the B.S. degree in electronics engineering from Kobe University, Hyogo, Japan, in 1990.

In 1990, he joined Electronics Research Laboratory of Matsushita Electronics Corporation in Osaka, where he was engaged in the research and development of GaAs MESFET and GaAs power module.



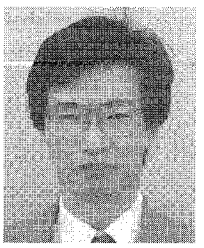
Hidetoshi Furukawa was born in Osaka, Japan. He received the B.S. and M.S. degrees in electronics engineering from the University of Osaka Prefecture, Osaka Japan, in 1984 and 1986, respectively.

In 1986, he joined Electronics Research Laboratory of Matsushita Electronics Corporation in Osaka, where he was engaged in the research and development of GaAs MESFET, HEMT, and MMIC. He is now working on the development of GaAs power FET which is used in the handheld phone set.



Noriyuki Yoshikawa was born in Nara, Japan. He received the B.S. degree in communication engineering from the University of Electro Communications, Tokyo, Japan, in 1983.

In 1983, he joined Electronics Research Laboratory of Matsushita Electronics Corporation in Osaka. Since then, he has been involved in the research and development of semiconductor devices, such as GaAs FET's and GaAs IC's.



Kunihiko Kanazawa was born in Kyoto, Japan. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Kyoto University, Kyoto, Japan, in 1979, 1981, and 1995, respectively.

In 1981, he joined Electronics Research Laboratory of Matsushita Electronics Corp. in Osaka. From 1981 to 1992, he worked on microwave integrated circuits and low noise FET's. Since 1992, he has been engaged in the research and the development of GaAs power amplifiers and MMIC's. He is currently the Manager of the Microwave Device Design Group.

Dr. Kanazawa is a member of the Institute of Electronics, Information and Communication Engineers in Japan.